Machine learning-based optimization of interleaver patterns for parallel concatenated block codes with arbitrary-length message blocks

Abstract

Parallel Concatenated Block (PCB) codes are a class of advanced error protection techniques. These codes employ two linear block codes, linked by an interleaver in the parallel form. The interleaver rearranges the position of original bits for a constituent block code, aiming to mitigate the effect of errors on the performance of the PCB code. Unlike other types of concatenated codes, such as product codes and Polar-Cyclic Redundancy Check (CRC) codes, PCB codes have a weaker error-correcting capability as some bits of the codeword are punctured. Regardless of this limitation, the parallel-based structure of PCB codes represents low complex and high-rate codes, making them attractive for the high-throughput-based applications. This design trade-off places greater emphasis on the interleaver. To date, PCB codes apply information, whose length is the square of the length of information considered for the constituent encoders. In this case, the minimum weight of the PCB code, represented as an important parameter for determining the error-correcting capability, is obtained from information with weight one. This research presents a novel permutation algorithm for the PCB code, whose length is multiple but not a square of the information length of the constituent codes, where the minimum weight of the PCB code from information with weight greater than one is expected. A machine learning-based approach using the Random Forest algorithm is adopted to optimize the permutation algorithm. Comparative simulations confirm that the PCB codes constructed by proposed interleavers outperform other well-known codes. This is evident for long-length based information.